

- TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMISSION DATA, C4 TO C0 SHOW CRC BITS)
- CONVENTIONAL POSTPOSITION : D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, C4, C3, C2, C1, C0
- PREPOSITION : C4, C3, C2, C1, C0, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0

FIG.1A

- RECEIVED DATA BIT AND RECEIVED CRC BIT  
(WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS  
SMALLER BY ONE FROM THE CORRECT RATE POSITION)
- CONVENTIONAL POSTPOSITION: DATA = D9, D8, D7, D6, D5, D4, D3, D2, D1 CRC=D0, C4, C3, C2, C1
- PREPOSITION: DATA = D9, D8, D7, D6, D5, D4, D3, D2, D1 CRC=C4, C3, C2, C1, C0

FIG.1B

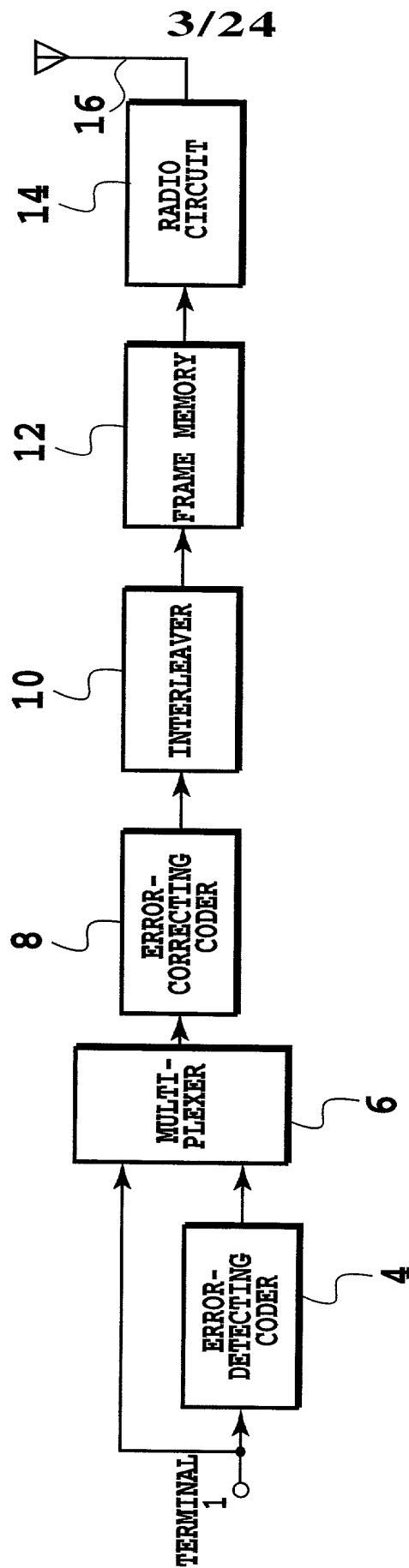
- TRANSMISSION BIT ORDER (D0 TO D9 SHOW TRANSMISSION DATA, C4 TO C0 SHOW CRC BITS)
- CONVENTIONAL POSTPOSITION: D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, C4, C3, C2, C1, C0
- NEW POSTPOSITION: D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, C0, C1, C2, C3, C4

FIG.2A

- RECEIVED DATA BIT AND RECEIVED CRC BIT  
(WHEN DETECTING A POSITION WHERE THE NUMBER OF BITS IS  
SMALLER BY ONE FROM THE CORRECT RATE POSITION)
- CONVENTIONAL POSTPOSITION: DATA = D9, D8, D7, D6, D5, D4, D3, D2, D1 CRC=D0, C4, C3, C2, C1
- NEW POSTPOSITION: DATA = D9, D8, D7, D6, D5, D4, D3, D2, D1 CRC=D0, C0, C1, C2, C3

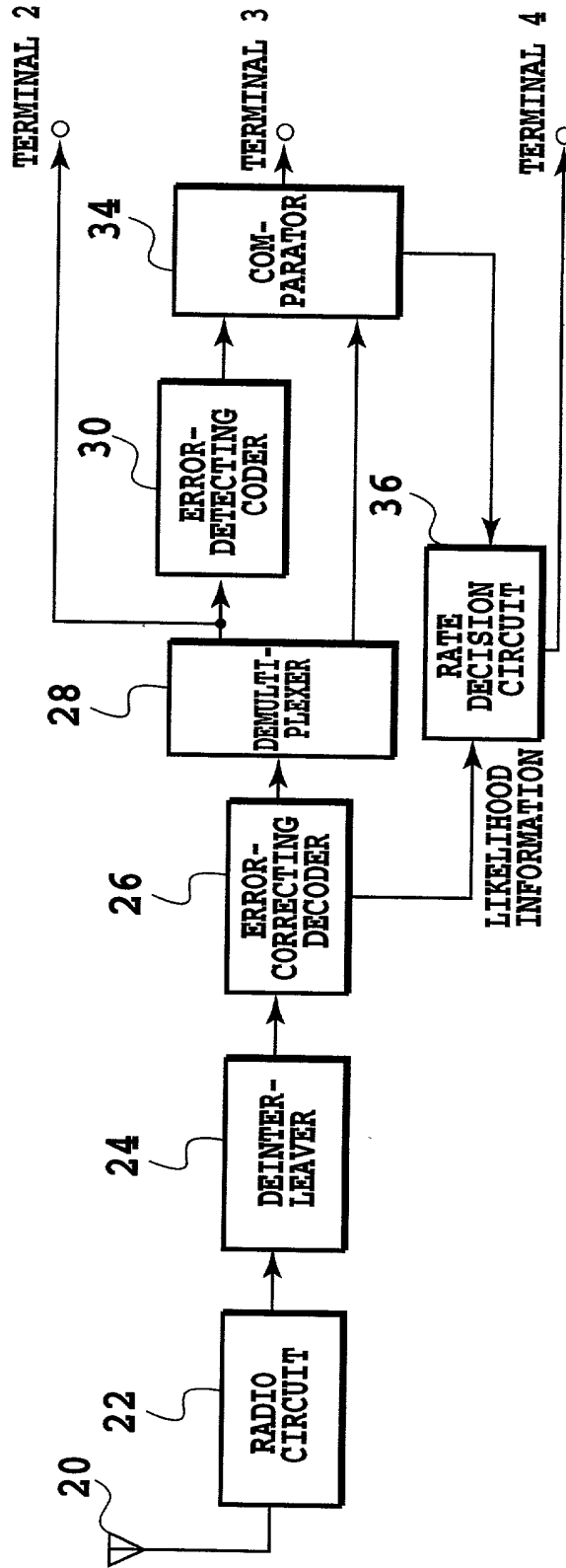
FIG.2B

FIG. 3A is a block diagram of a transmitter configuration. The transmitter includes a terminal 1, an error detecting coder 4, a multi-plexer 6, an error correcting coder 8, an interleaver 10, a frame memory 12, and a radio circuit 14. The terminal 1 is connected to the error detecting coder 4. The error detecting coder 4 is connected to the multi-plexer 6. The multi-plexer 6 is connected to the error correcting coder 8. The error correcting coder 8 is connected to the interleaver 10. The interleaver 10 is connected to the frame memory 12. The frame memory 12 is connected to the radio circuit 14. The radio circuit 14 is connected to an antenna 16. The antenna 16 is connected to a power source 3/24.



TRANSMITTER CONFIGURATION

FIG.3A



RECEIVER CONFIGURATION

FIG.3B

OUTPUT OF MULTIPLEXER

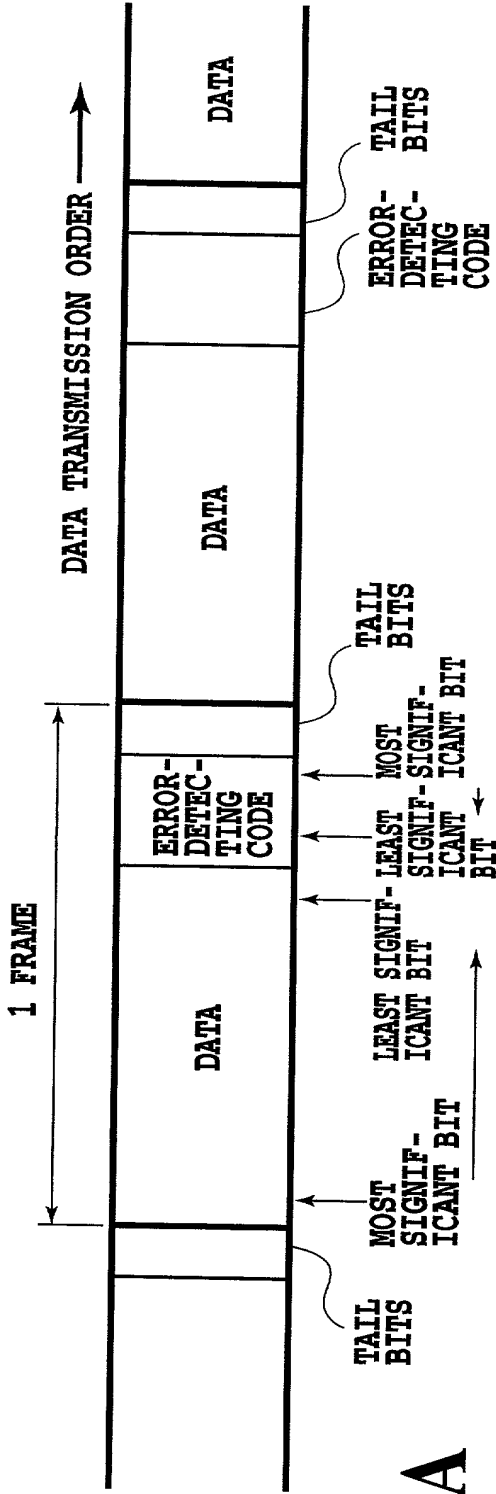


FIG. 4A

OUTPUT OF MULTIPLEXER

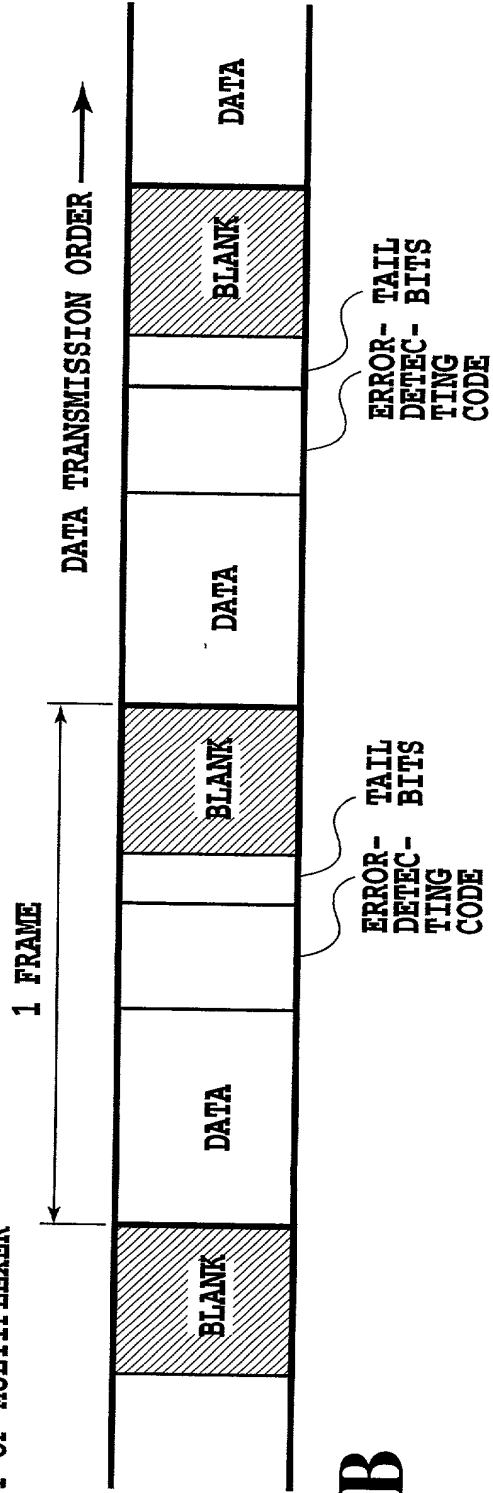


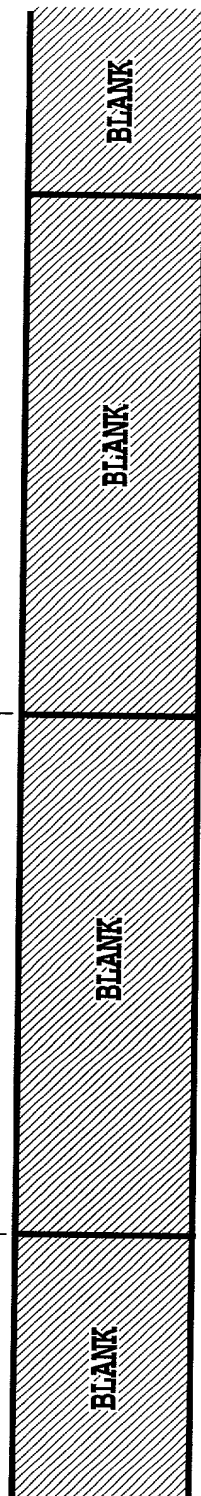
FIG. 4B

1. The first step in the process is to determine the total number of channels to be multiplexed. This is done by counting the number of channels that are to be transmitted simultaneously.

OUTPUT OF MULTIPLEXER

1 FRAME

DATA TRANSMISSION ORDER →



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FIG.4C

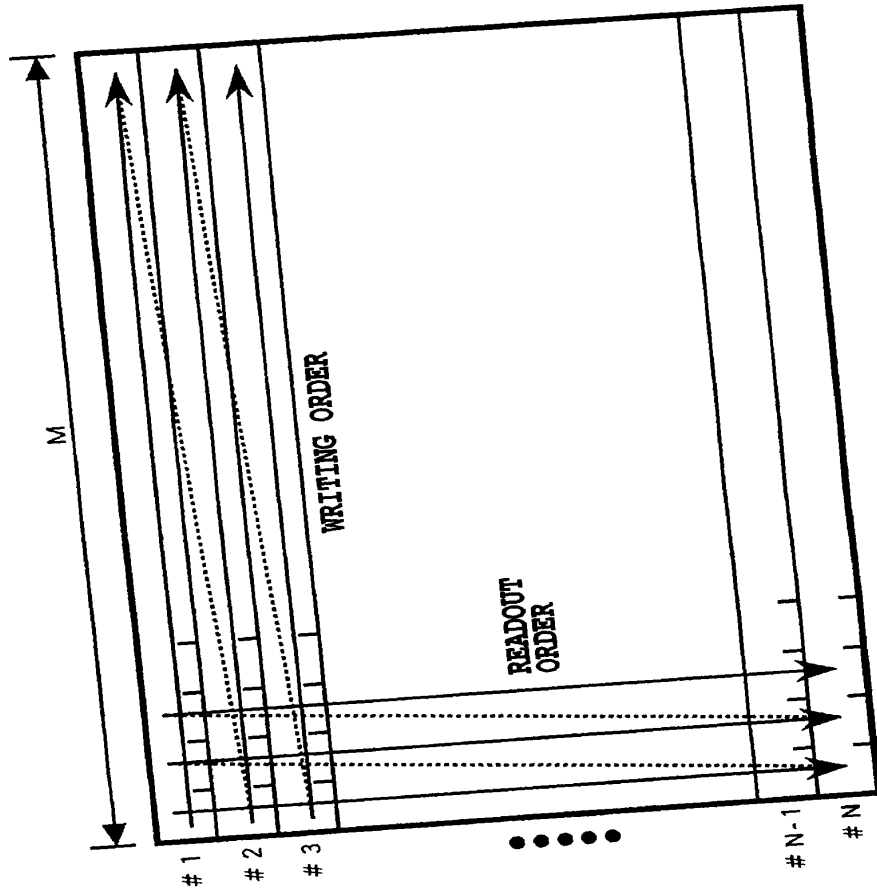


FIG.5

Page 1 of 1  
Date: 10/10/2019  
Time: 10:10:10  
User: admin

# OUTPUT OF FRAME MEMORY

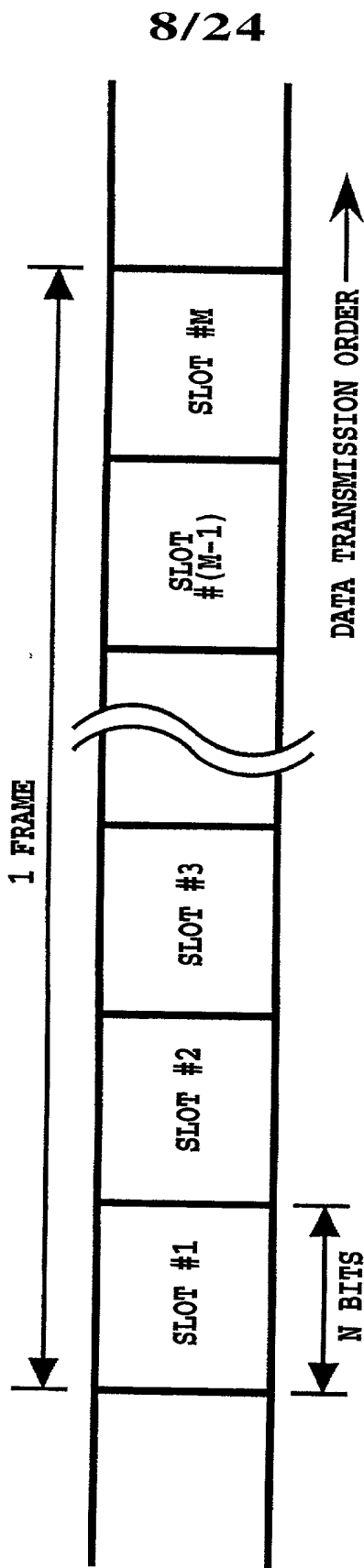


FIG.6



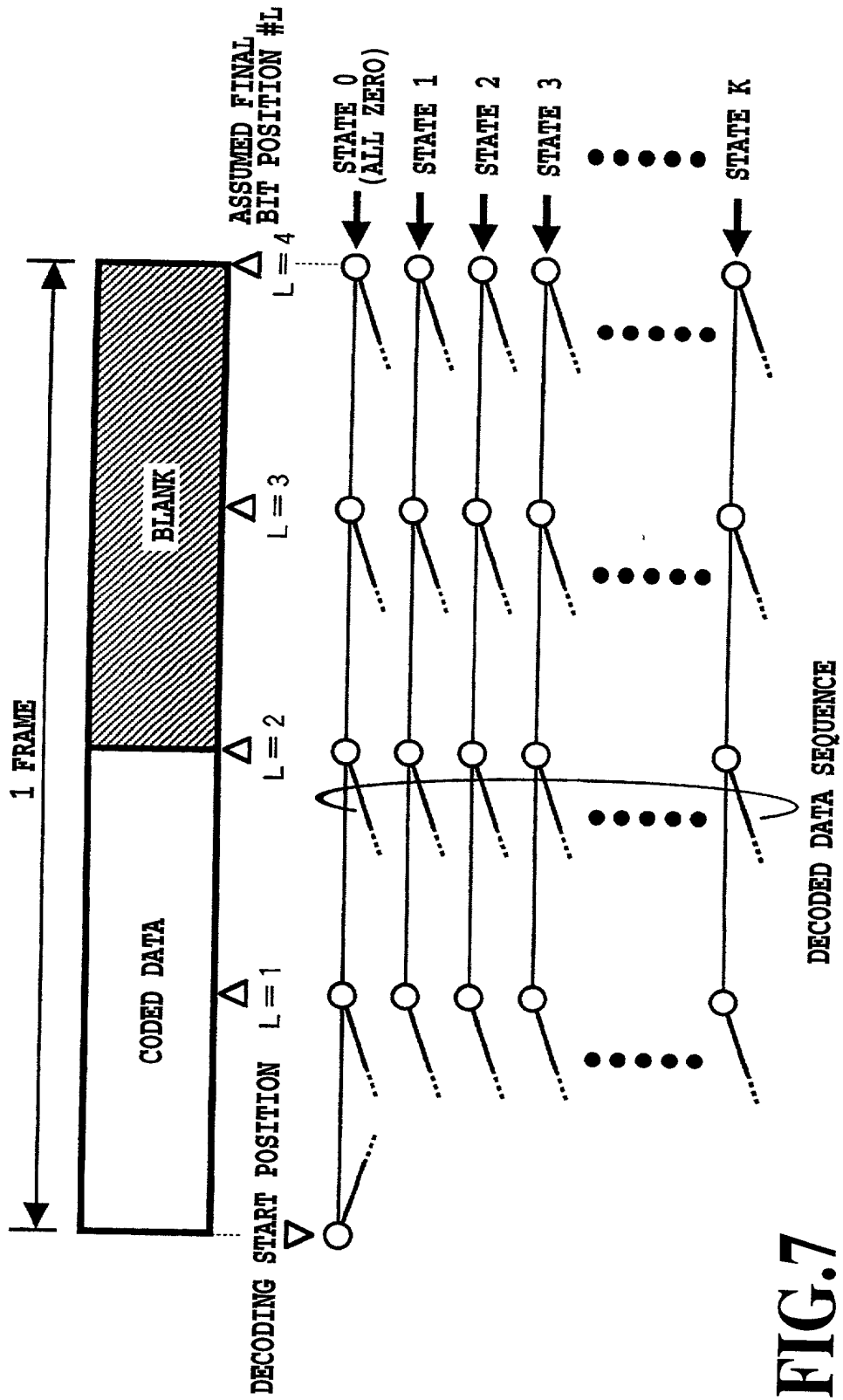


FIG.7

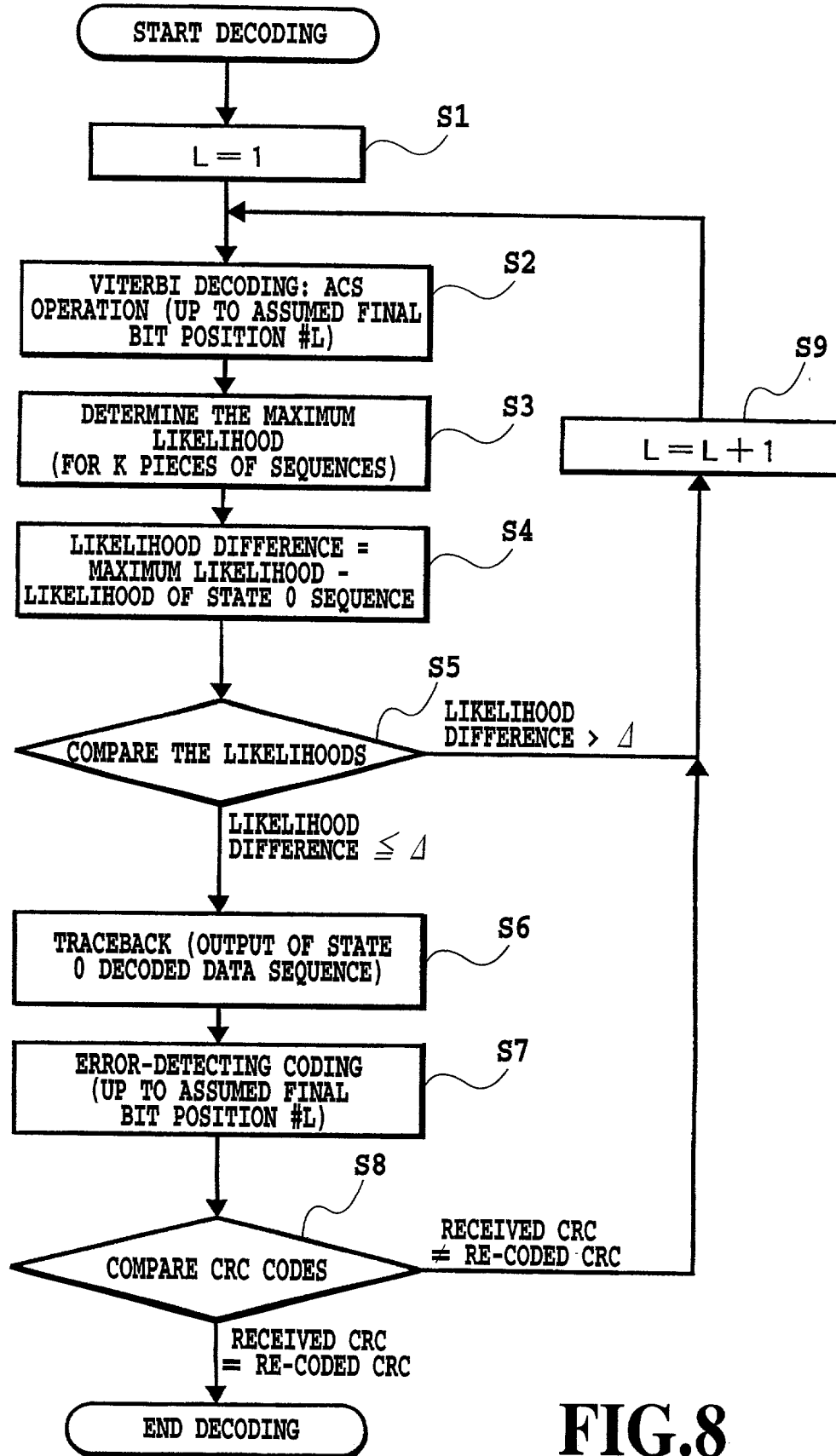


FIG.8

FIG. 9A

START DECODING

S21  
 $L = 1$   
 $S_{min} = \Delta$   
 $L' = -1$

S22  
VITERBI DECODING: ACS OPERATION  
(UP TO ASSUMED FINAL  
BIT POSITION #L)

S23  
DETERMINE THE MAXIMUM LIKELIHOOD  
(FOR K PIECES OF SEQUENCES)

S24  
LIKELIHOOD DIFFERENCE  $S(L) =$   
MAXIMUM LIKELIHOOD -  
LIKELIHOOD OF STATE 0 SEQUENCE

S25  
COMPARE THE LIKELIHOODS  
 $S(L) \leq \Delta$   
 $S(L) > \Delta$

S32  
 $L = L + 1$

S31  
IS L THE MAXIMUM ?  
Yes  
No

S33  
MAKE DECISION THAT  
POSITION L' IS FINAL  
BIT POSITION

END DECODING

FIG. 9

FIG. 9A

FIG. 9A

FIG. 9B

FIG. 9B

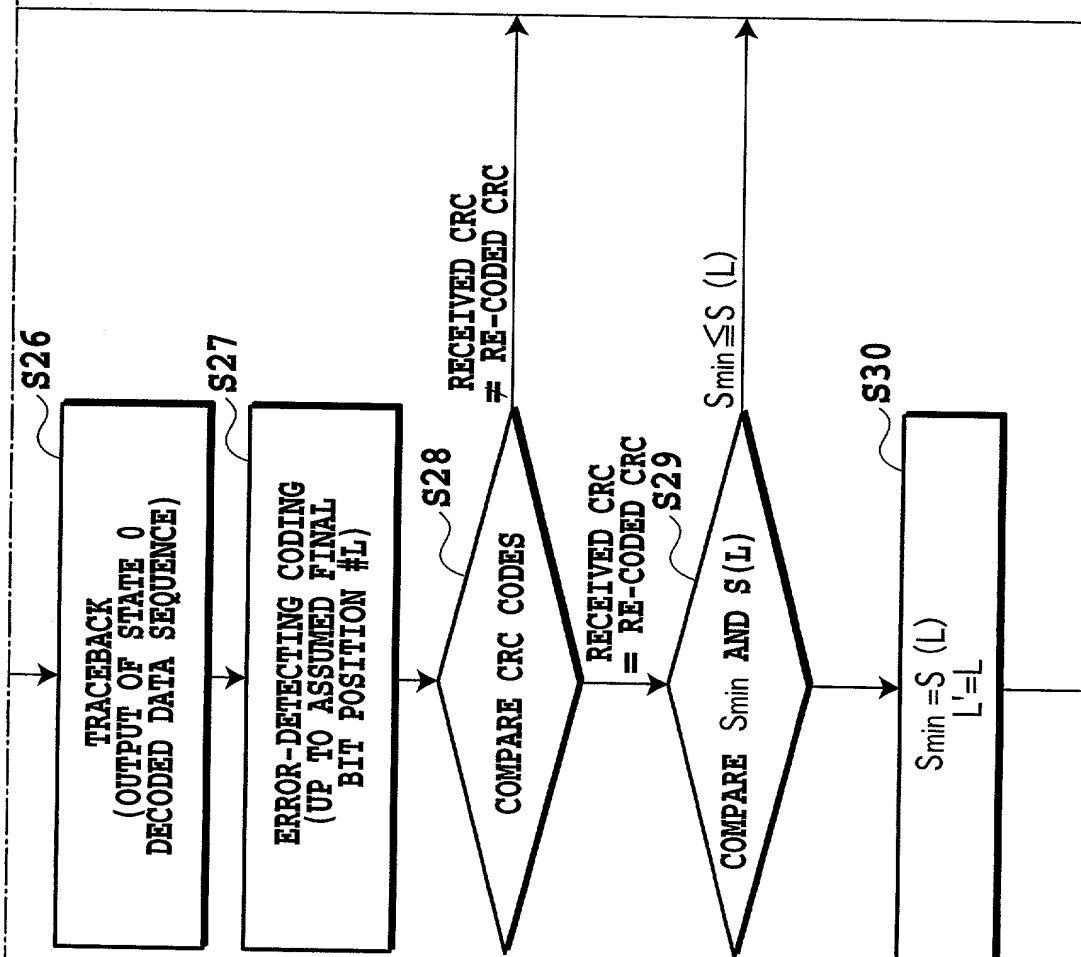
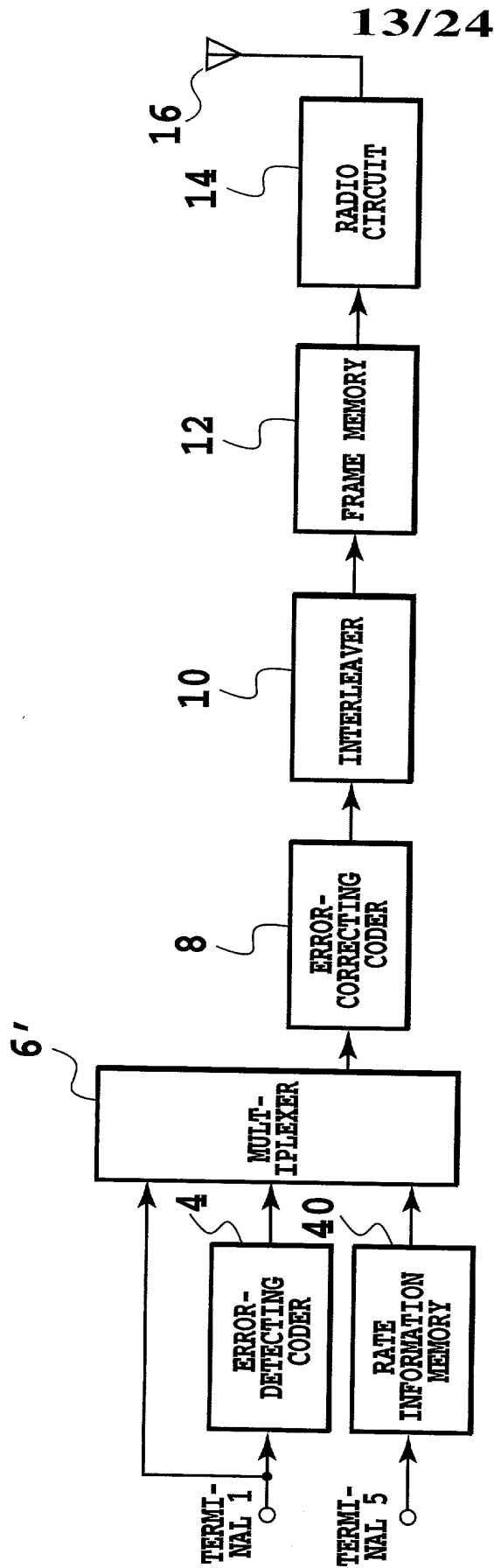


FIG. 10A is a block diagram of a transmitter configuration. The transmitter includes a terminal 1, a terminal 5, an error detecting coder 4, a rate information memory 40, a multiplexer 6', an error correcting coder 8, an interleaver 10, a frame memory 12, a radio circuit 14, and an antenna 16. The terminal 1 and terminal 5 are connected to the error detecting coder 4. The error detecting coder 4 is connected to the multiplexer 6'. The rate information memory 40 is connected to the multiplexer 6'. The multiplexer 6' is connected to the error correcting coder 8. The error correcting coder 8 is connected to the interleaver 10. The interleaver 10 is connected to the frame memory 12. The frame memory 12 is connected to the radio circuit 14. The radio circuit 14 is connected to the antenna 16. The antenna 16 is labeled 13/24.



TRANSMITTER CONFIGURATION

FIG.10A

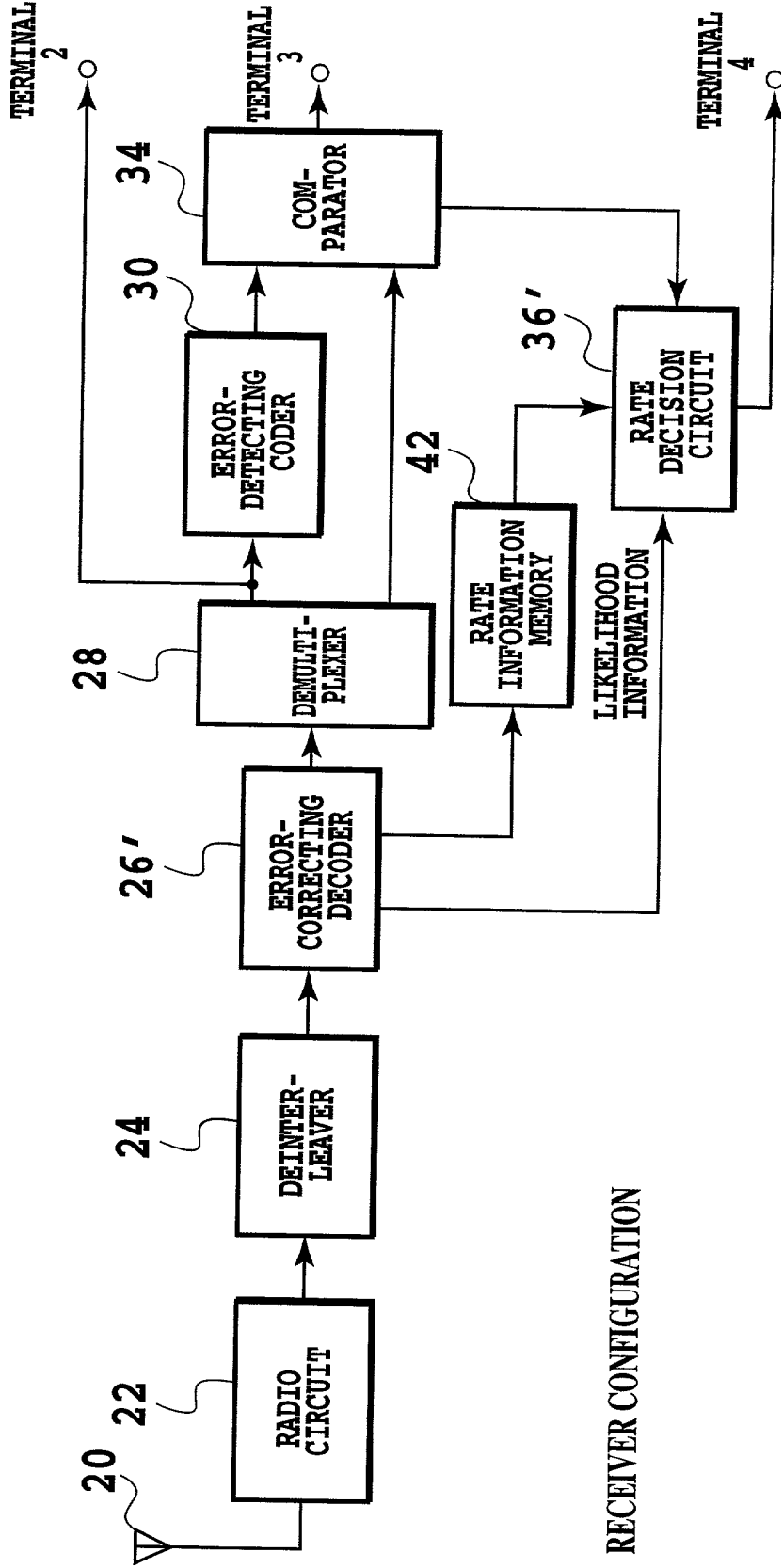


FIG.10B

OUTPUT OF MULTIPLEXER

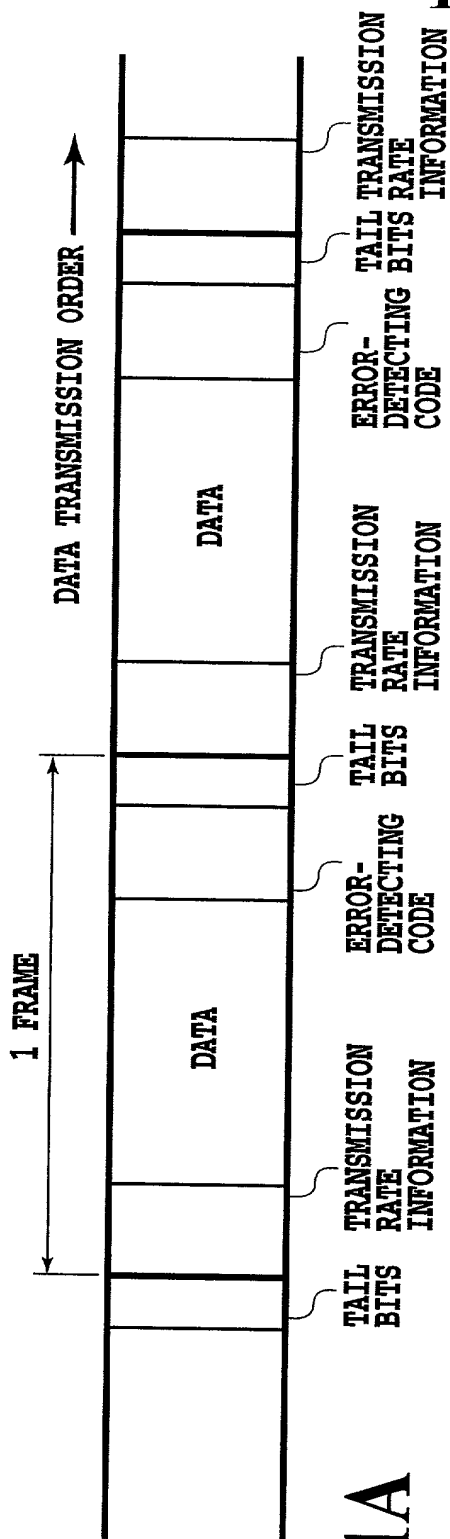


FIG. 11A

OUTPUT OF MULTIPLEXER

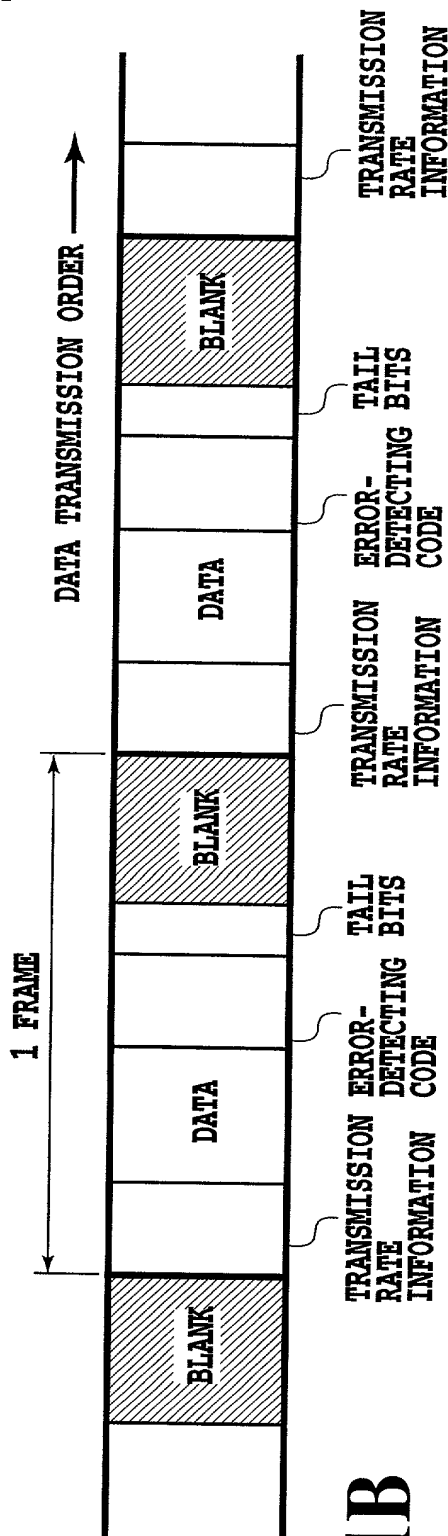


FIG. 11B

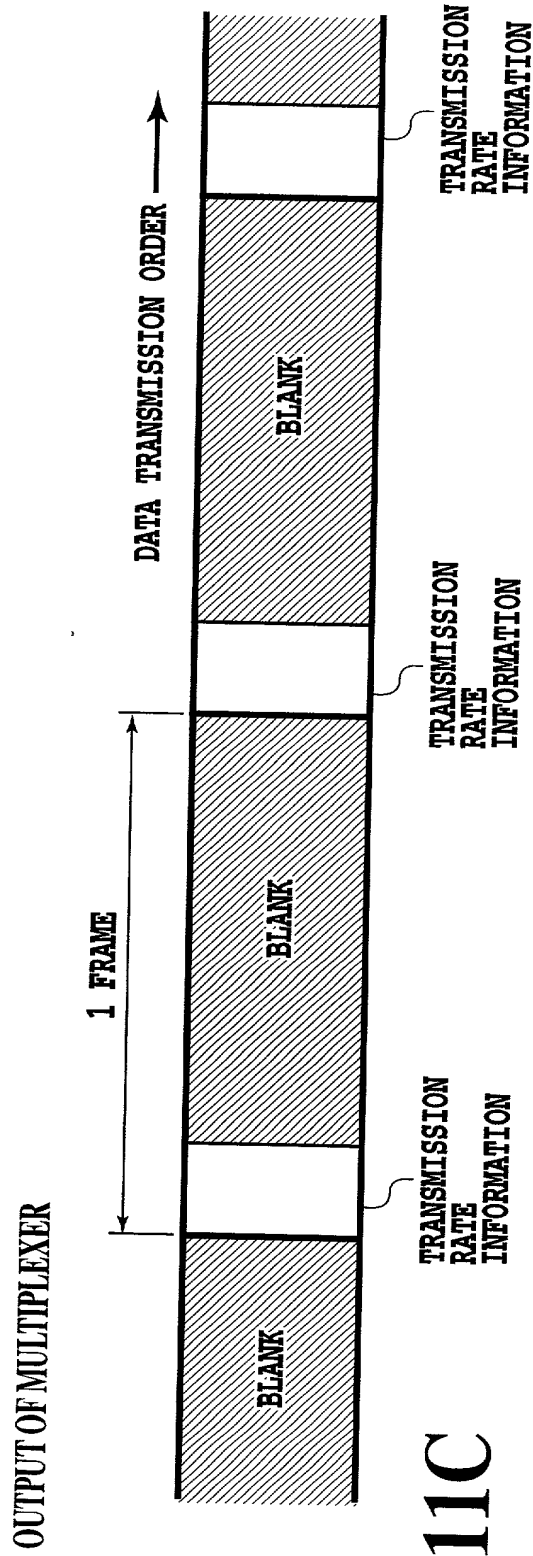


FIG.11C



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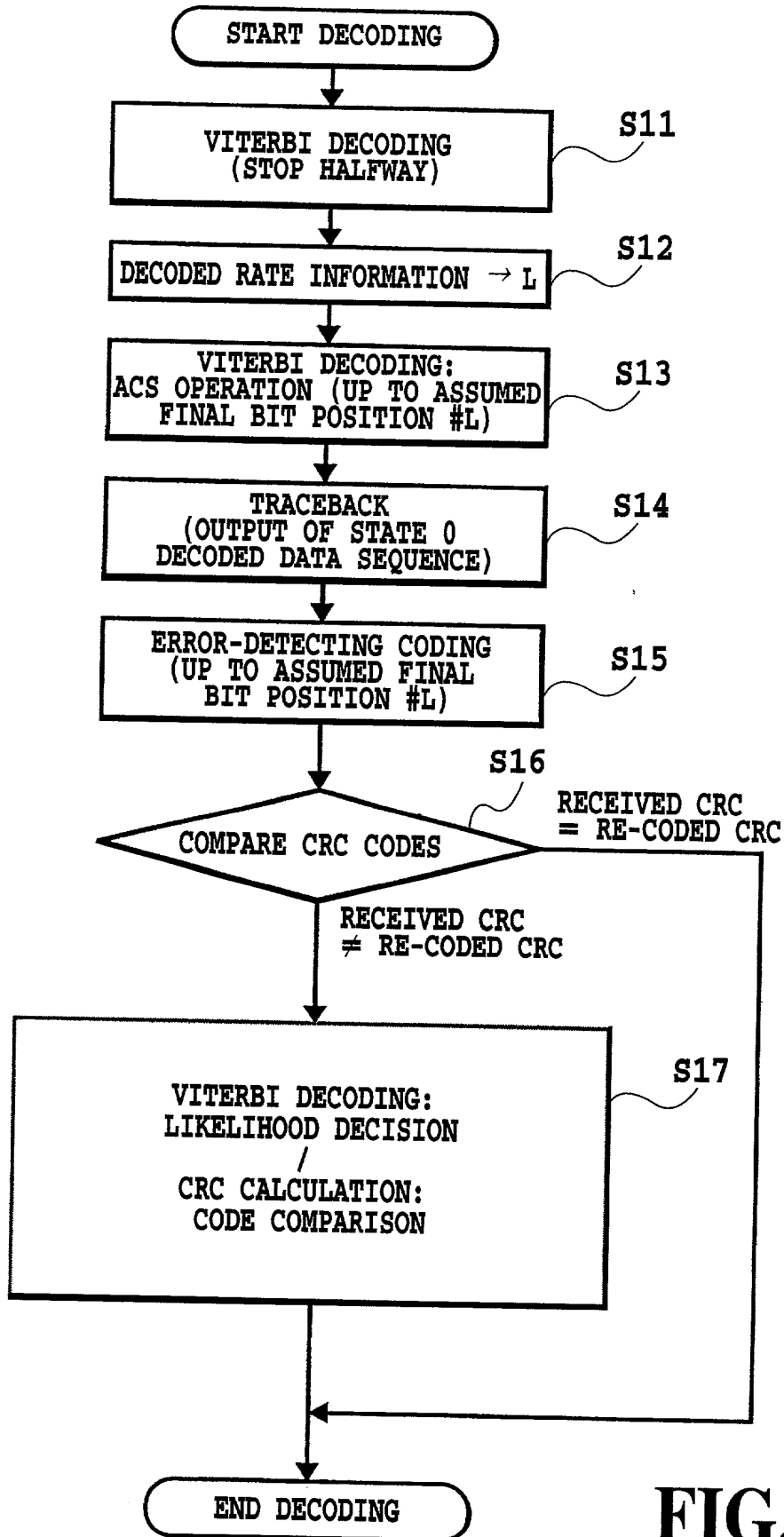
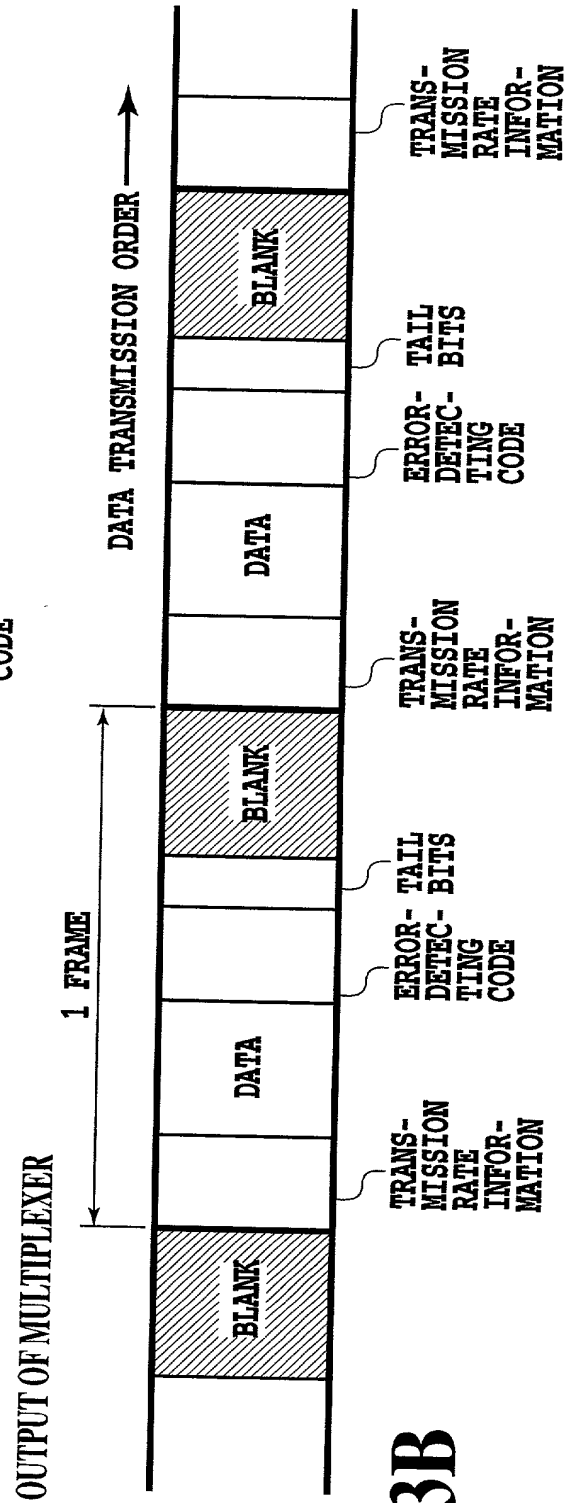
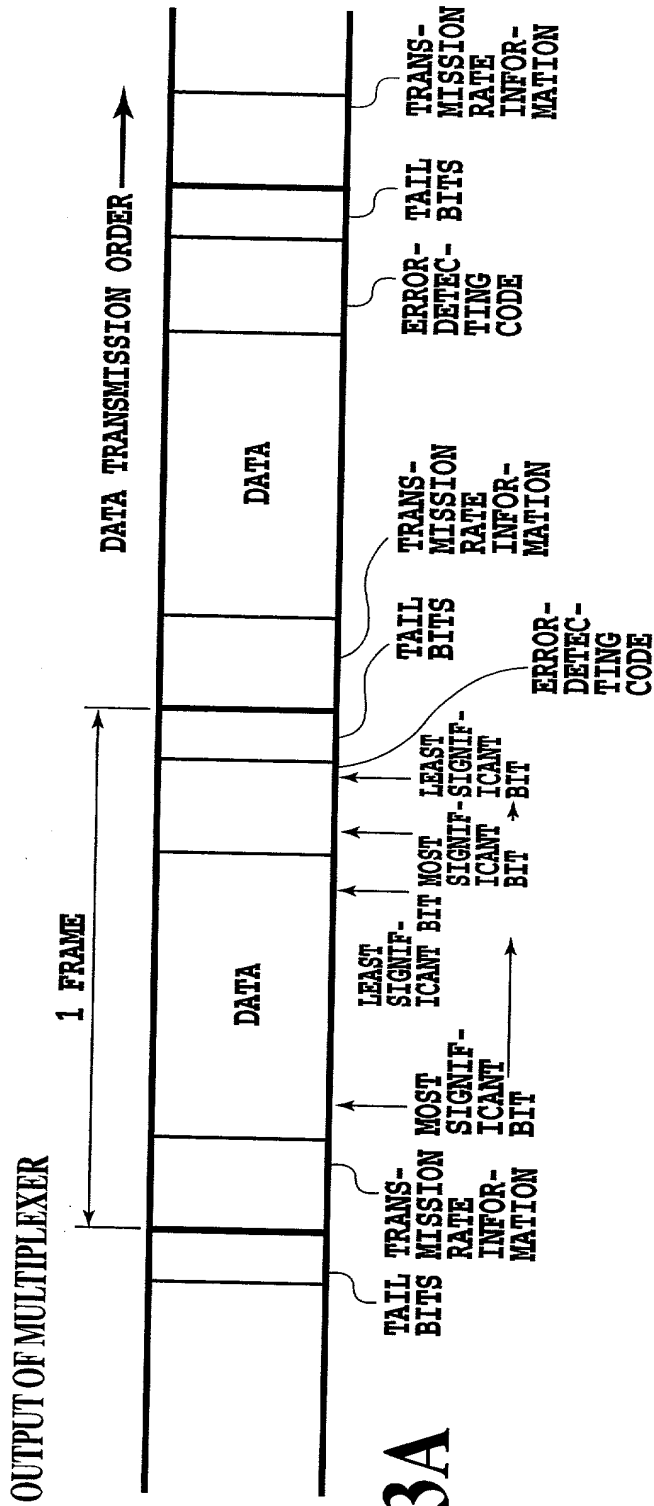


FIG.12



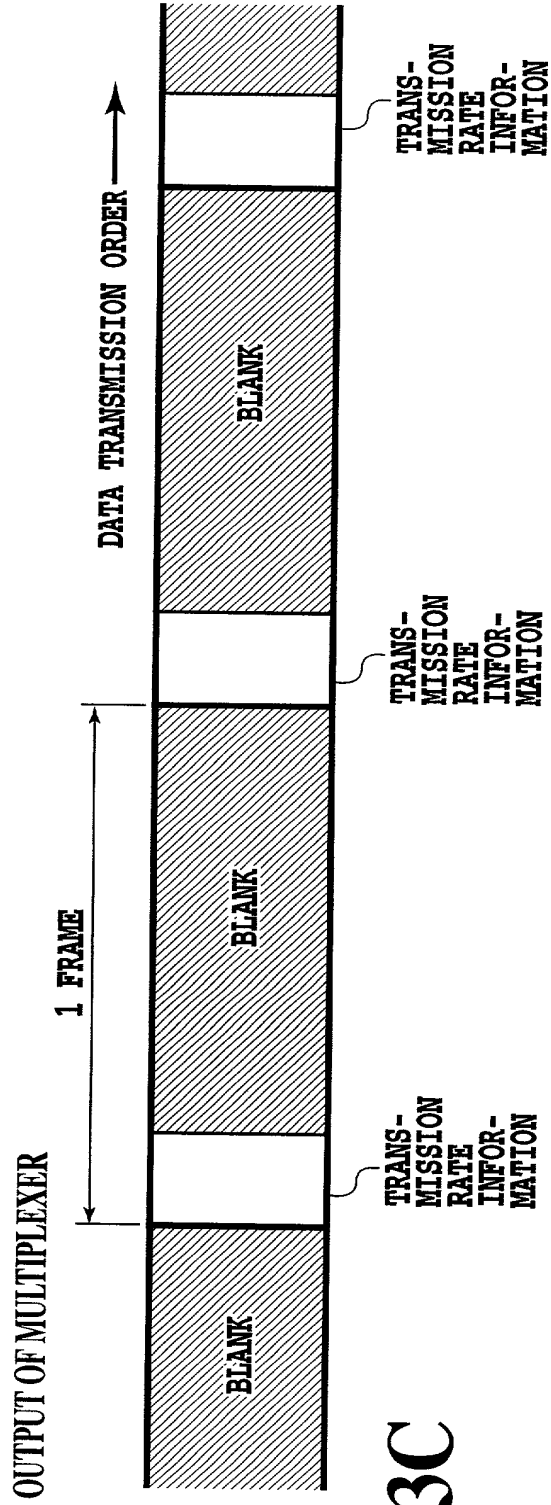


FIG.13C

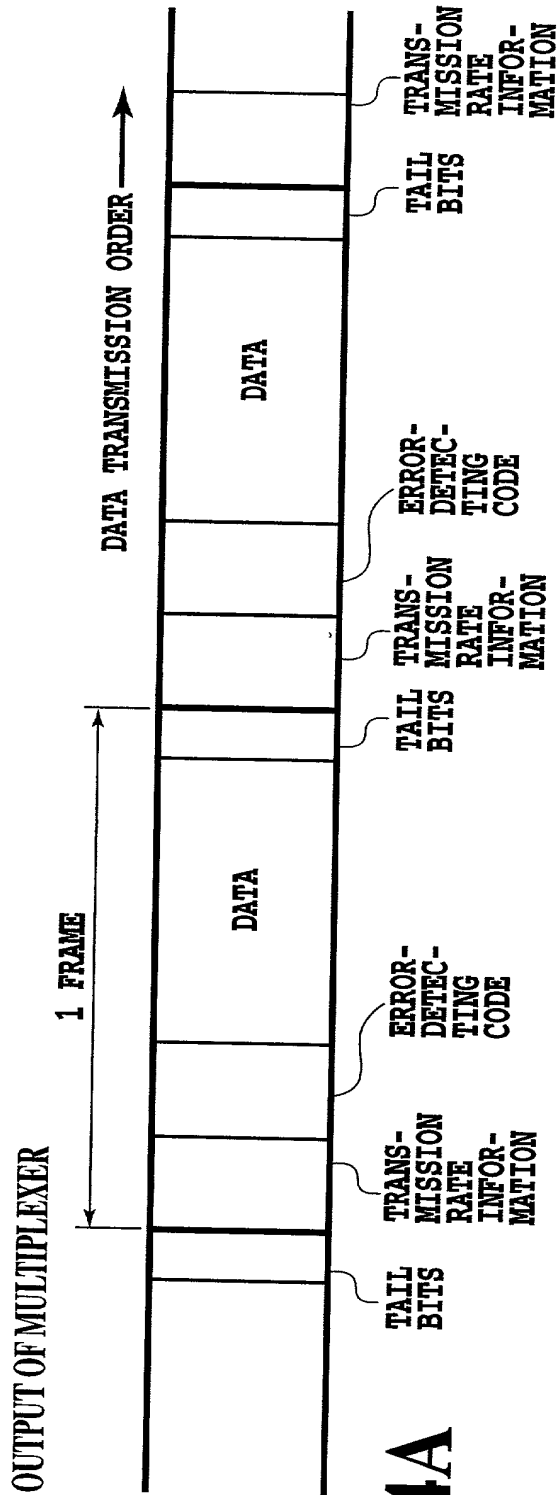


FIG.14A

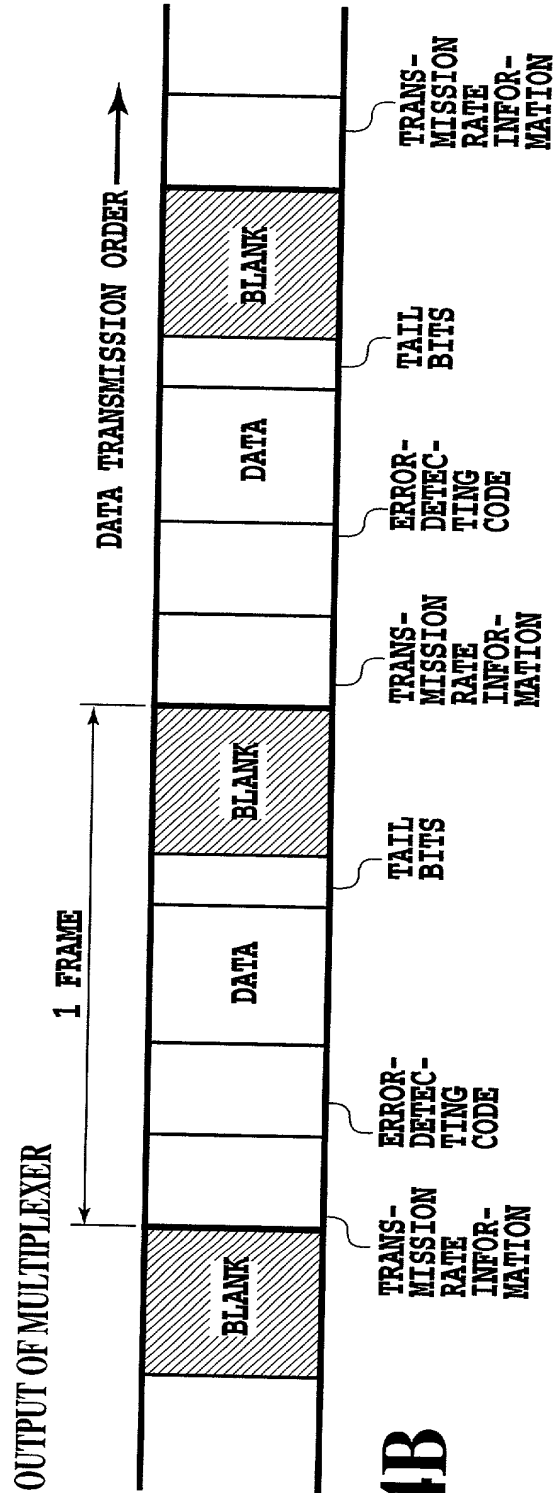


FIG.14B

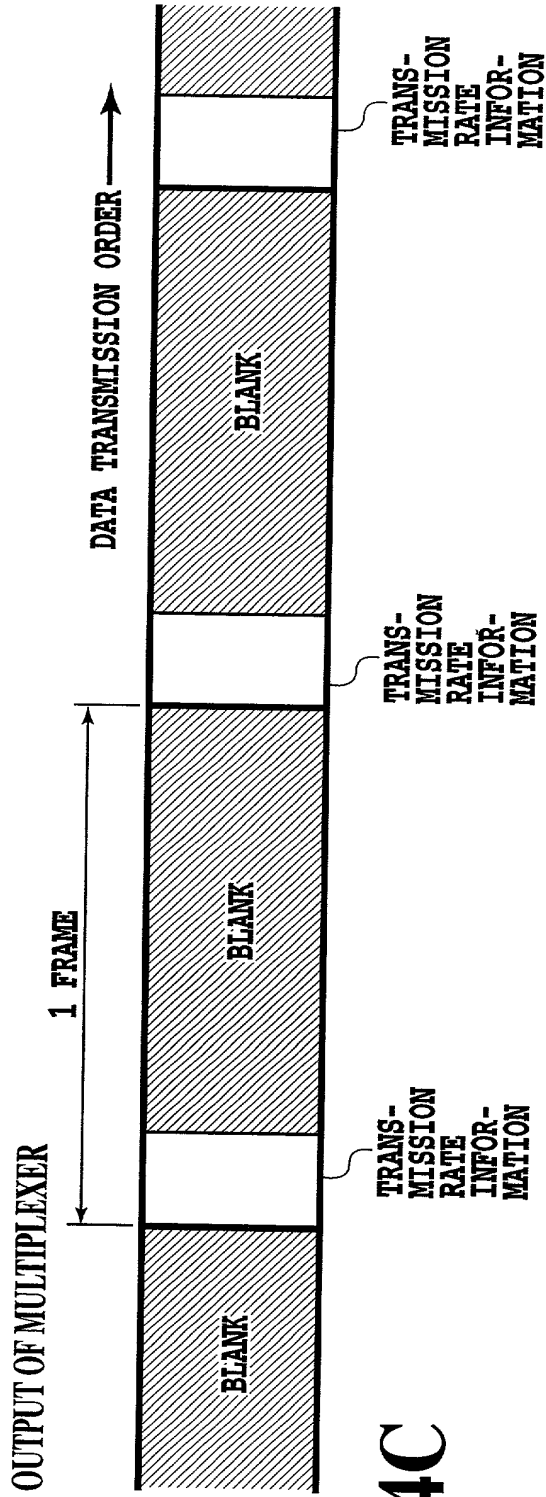
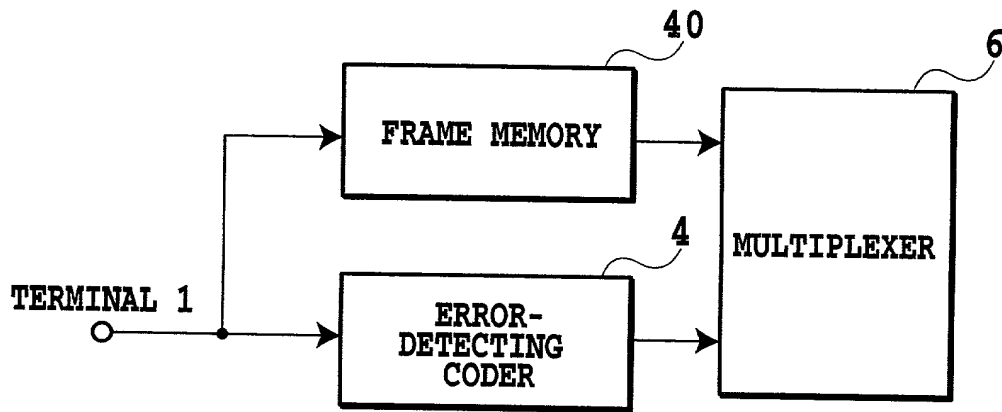
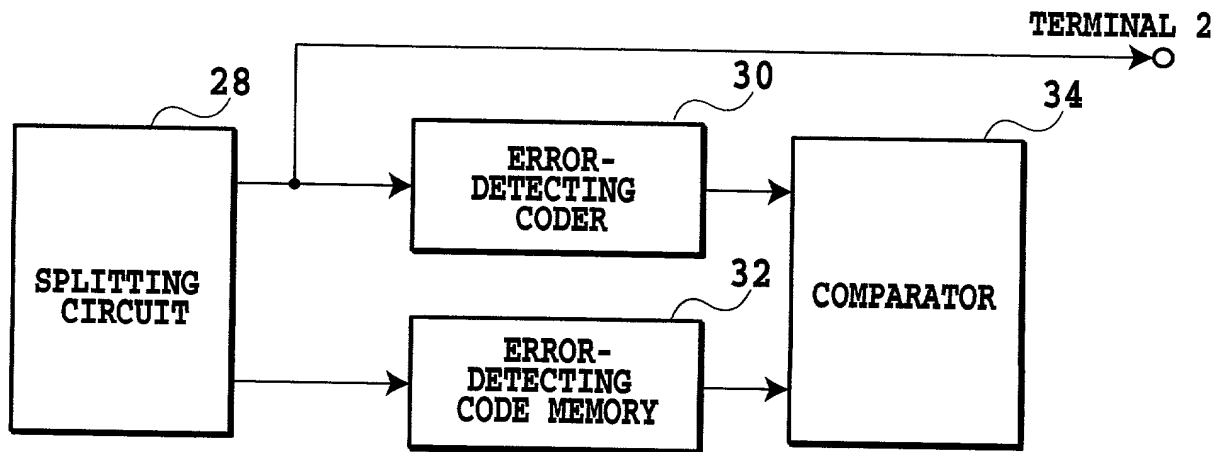


FIG. 14C



**FIG.15A**



**FIG.15B**

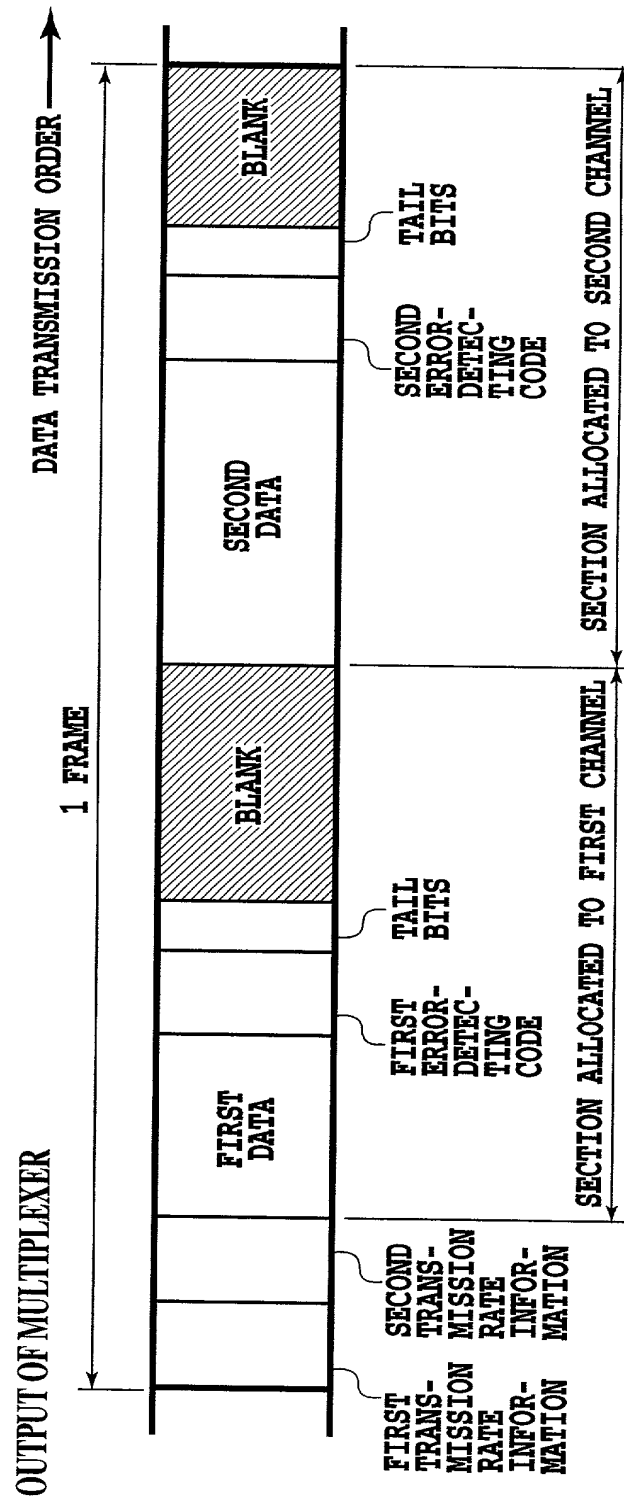


FIG.16

output of the multiplexer is a stream of bits which are transmitted in the following order: first data, first error-detecting code, tail bits, blank, second data, second error-detecting code, tail bits, blank.

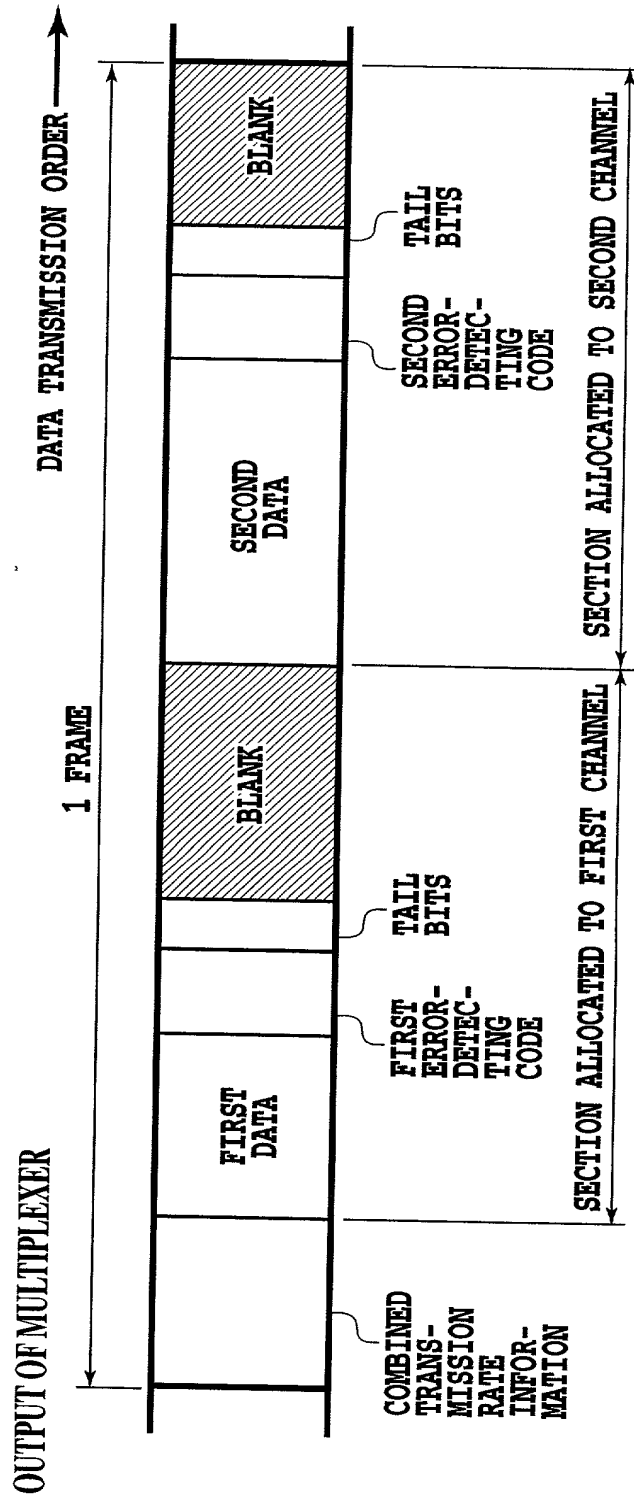


FIG.17